UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,352	07/14/2005	Juha Paaso	3003-00048	1665

26753 7590 05/23/2008

ANDRUS, SCEALES, STARKE & SAWALL, LLP
100 EAST WISCONSIN AVENUE, SUITE 1100
MILWAUKEE, WI 53202

EXAMINER	
AMINI, JAVID A	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
05/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,352	PAASO, JUHA	
	Examiner	Art Unit	
	JAVID A. AMINI	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toriya et al. 6867769, hereinafter Toriya, and in view of Gorman et al. 6798411, hereinafter Gorman.

1.

Toriya teaches a method for processing a computer aided polygon model (e.g., noted in figs. 9), comprising: Toriya teaches forming a linear vertex array which is static and which contains the vertices of the image elements of the polygon model (e.g., noted in fig. 11 steps 1-3); Toriya teaches forming a linear index array whose elements define the image elements of the polygon model by pointing at the vertices of each image element, and which linear index array comprises an active part, the image elements defined by the elements of the active part being included in the polygon model part to be presented graphically (e.g., noted in col. 2 lines 37-46, examiner's interpretation: the matched vertex of Toriya may be similar to what in the claim language recited as "active part");

However, the second reference Gorman teaches explicitly the linear index array comprises an active part, because in fig. 6 after creating the mesh 112, the software 110 then

uses mesh reduction techniques to simplify the mesh. A wide variety of mesh reduction techniques can be used such as edge-collapsing, vertex clustering, and/or vertex decimation. After simplification, the software 110 encodes the mesh for later reconstruction into an image, examiner believes, e.g., the vertex decimation would keep the active element of the model. and by using a vertex calculation unit 10 of Toriya in col. 4 lines 25-32 obviously modifying the active part of the index array to change the image elements included in the polygon model part to be presented graphically while maintaining the linearity of the index array (e.g., in fig. 18b).

Thus, it would have been obvious to a person skill in the art at the time of the invention to combine Gorman into Toriya, in order to minimize the size of an image for nearly half-a-million pixels. The large amount of data needed to describe each pixel in an image can consume a lot of space on a computer hard disk or take a long time to download over a network. Thus, it would be advantageous to develop a technique for reducing the amount of data needed to represent an image.

2.

A method according to claim 1, further comprising presenting graphically the polygon model part to be presented graphically, see figs. 9, 14 and 18.

3.

A method according to claim 1, further comprising modifying the active part of the linear index array by replacing an element of the linear index array with another element of the linear index array (e.g., in fig. 2 #102f is replaced or modified with #102i in fig. 4 of Gorman).

4.

A method according to claim 1, further comprising forming the linear vertex array in such a way that each vertex appears in the vertex array only once (e.g., Toriya in figs. 13 teaches each vertex appears in the vertex array only once).

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toriya and Gorman, and further in view of Mortlock et al. 6549200, hereinafter Mortlock.

5.

Toriya and Gorman do not explicitly specify a method according to claim 1, further comprising forming a linear index array in such a way that the linear index array further comprises a passive part, the image elements defined by the elements of the passive part belonging to the outside of the polygon model part to be presented graphically; and modifying the active part of the linear index array by moving at least one element of the linear index array between the active part and the passive part,

However, Mortlock teaches forming a linear index array in such a way that the linear index array further comprises a passive part, the image elements defined by the elements of the passive part belonging to the outside of the polygon model part to be presented graphically; and modifying the active part of the linear index array by moving at least one element of the linear index array between the active part and the passive part, e.g., in bridging paragraph cols. 5-6 specify providing animation of a mouth, i.e. considered as an active part of the face.

Thus, it would have been obvious to a person skill in the art at the time of the invention to combine Mortlock into Gorman and Toriya, in order to determine co-ordinates of the vertices of the surface element with respect to a co-ordinate system corresponding to the directions of

view, and determining the maximum difference in the co-ordinates in each of the directions of view, and forming ratios of the maximum differences with respect to each direction of view.

6.

Toriya teaches a method according to claim 1, further comprising registering the modification of the linear index array in such a way that the linear index array is restorable to the state preceding the modification (e.g., in fig. 13a shows the index of lattice polygon model with surface model are stored and obviously after modification of control points in fig. 13c, the index in fig. 13A is restorable).

7.

Claims 7-8, 13-16, 21-24 are rejected with similar reasons as set forth in claim 5, above.

Claims 9-12, 17-20 are rejected with similar reasons as set forth in claims 1-4, respectively, above.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 17-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter as follows. Claims 17-24 define a [a computer program,] embodying functional descriptive material. However, the claim does not define a computer-readable medium or memory and is thus non-statutory for that reason (i.e., "When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally

interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized" – Guidelines Annex IV). That is, the scope of the presently claimed [a computer program] can range from paper on which the program is written, to a program simply contemplated and memorized by a person. The examiner suggests amending the claim to embody the program on "computer-readable medium" or equivalent in order to make the claim statutory. Any amendment to the claim should be commensurate with its corresponding disclosure.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-24 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-12 of copending Application No. 10/593673. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

Current 10/542352	Copending 10/593673
1. A method for processing a computer aided polygon model, comprising: forming a linear vertex array which is static and which contains the vertices of the image elements of the polygon model; forming a linear index array whose elements define the image elements of the polygon model by pointing at the vertices of each image element, and which linear index array comprises an active part, the image elements defined by the elements of the active part being included in the polygon model part to be presented graphically; and modifying the active part of the index array to change the image elements included in the polygon model part to be presented graphically while maintaining the linearity of the index array. 2. A method according to claim 1, further comprising presenting graphically the polygon model part to be presented graphically. 3. A method according to claim 1, further comprising modifying the active part of the linear index array by replacing an element of the linear index array with another element of the linear index array. 4. A method according to claim 1, further comprising forming the linear vertex array in such a way that each vertex appears in the vertex array only once. 5. A method according to claim 1, further comprising forming a linear index array in such a way that the linear index array further comprises a passive part, the image elements defined by the elements of the passive part belonging to the outside of the polygon model part to be presented graphically; and modifying the active part of the linear index array by moving at least one element of the linear index array between the active part and the passive part. 6. A method according to claim 1, further comprising	1. A method for processing a computer aided polygon model, comprising: forming (502) a vertex array which is linear and static and comprises the vertices of the image elements of the polygon model; forming (504) an index array which is linear and the elements of which determine the image elements of the polygon model by pointing at the vertices of the image elements in the vertex array, and which index array comprises an active part, the image elements determined by the elements of the active part being included in the polygon model part to be presented graphically; characterized by forming (506) additionally a hierarchical data structure whose hierarchy is based on the division of the vertices in the image space, the nodes of which hierarchical data structure point at nodes of a lower level in the hierarchy, the leaf nodes of the hierarchical data structure pointing at elements of the active part of the index array; and reducing (510) the polygon model part to be presented graphically by means of the hierarchical data structure, maintaining the linearity of the index array.

registering the modification of the linear index array in such a way that the linear index array is restorable to the state preceding the modification. 7. A method according to claim 1, further comprising receiving a modification command to modify the active part of the linear index array; and changing the size of the active part of the linear index array on the basis of the modification command.	
8. A method according to claim 1, further comprising receiving a modification command to modify the active part of the linear index array; and modifying the active part of the linear index array on the basis of the modification command.	2. A method according to claim 1, characterized by reducing (510) the polygon model by removing (602) at least two hierarchically equal leaf nodes from the hierarchical data structure; including (604) the location information representing the vertices pointed at by the index array elements pointed at by said at least two leaf nodes in a node of an upper level in the hierarchy, whereby this upper level node becomes a leaf node; and removing (606) at least one element of the index array pointed at by said at least two hierarchically equal leaf nodes from the active part.
	3. A method according to claim 1, characterized by forming (504) an index array in such a way that the index array also comprises a passive part, the vertices pointed at by the elements of the passive part belonging outside the polygon model part to be presented graphically; and reducing (510) the polygon model part by moving at least one index array element from the active part to the passive part.
	4. A method according to claim 1, characterized by forming (506) a hierarchical data structure by: dividing (702) the coordinate space represented by the polygon model into hierarchical sectors on the basis of vertices contained in the vertex array; including (704) the pointers of the nodes corresponding to the sectors of the next lowest level in the hierarchy in the node corresponding to each hierarchical sector; including (706) the pointers pointing at the index array elements pointing at the vertices determining the lowest hierarchical sector in the leaf nodes.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending

application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAVID A. AMINI whose telephone number is (571)272-7654. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Javid A Amini
Primary Examiner
Art Unit 2628

/Javid A Amini/
Primary Examiner, Art Unit 2628